first error detecting means or the second error detecting means detects an error-containing code word;

a stored code calculation selecting means for selecting between the first syndrome calculating means and the second syndrome calculating means in ECC block units or in said data units so as to perform syndrome calculation for the data stored in said buffer memory;

a parallel transfer means for, on and after the second-time error correction in a same direction, before the first syndrome calculating means detects an error-containing code in said data units, transferring code words not stored in said storing means out of data stored in said buffer memory to the corresponding one of the first syndrome calculating means and the first error detecting means;

a second-time onward detecting-processed data use means for, on and after the second-time error detection in the same direction done by the corresponding error detecting means, performing error detection of the subsequent code words in said data units by using the mid-term results stored in said storing means;

a means-basis pipeline processing notification means for transmitting ECC blocks which have been subjected to error correction downstream; for storing ECC blocks to be processed next to said buffer memory; and for making the storage known to said stored code calculation selecting means, said buffer memory parallel transfer means, said error-detecting-means switch means, the first syndrome calculating means, the second syndrome calculating means, said error detecting means, said error correcting means, said parallel transfer means, and said second-time onward

detecting-processed data use means; and

a system control means for controlling a data transfer and data rewriting of ECC blocks in process in ECC block units or said data units at each means and for coordinating with other means the transfer of error-corrected ECC blocks downstream and the storage of new ECC blocks to be processed in said buffer memory.

31. The error correction device of claim 1, 2, 3, 4, 5, 6, 7, 8, 28, 29, or 30 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

32. The error correction device of claim 9 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction

and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

33. The error correction device of claim 10 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error correction alternately in units of said predetermined capacity.

34. The error correction device of claim 11 further comprising:

two buffer memories each having a predetermined capacity equivalent to one sector or one ECC block;

a buffer memory storage means for alternately storing in said two buffer memories, in accordance with error correction speed, continuous data of the predetermined capacity which are a target of error correction and have been read from a DVD or a CD-ROM; and

an accessed buffer memory switch means for switching between said two buffer memories in order to read or write data as a target of error